REMARKS

In view of the above amendments and following remarks, reconsideration and further examination are requested.

The specification and abstract have been reviewed and revised to make editorial changes thereto and generally improve the form thereof, and a substitute specification and abstract are provided. No new matter has been added by the substitute specification and abstract. Also, enclosed is a "marked-up" copy of the original specification and abstract to show changes that have been incorporated into the substitute specification and abstract. The attached pages are captioned ***"Version with Markings to Show Changes Made."***

The Examiner objected to Figure 12 as not being labeled as --Prior Art--. Accordingly, provided herewith is a proposed drawing amendment, and formal drawing, for Figure 12 which labels this figure as --Prior Art--. Also, provided are proposed drawing amendments and Formal Drawings for Figures 6, 7A, 7B, 10, 11A and 11B to make these figures consistent with the written description thereof.

The Examiner rejected claims 4 and 11 under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim subject matter which Applicants regard as the invention. Specifically, the Examiner objected to the use of the phrase "different kind". By the current Amendment, claims 1-26 have been replaced by new claims 27-55. New claims 31 and 38, which generally correspond to originally filed claims 4 and 11, respectively, do not use the phrase "different kind", by rather recite that the semiconductors are --different-- from one another. This language is believed to be definite and in accordance with 35 U.S.C. 112, second paragraph, and the claims are otherwise believed to be in compliance with 35 U.S.C. 112, second paragraph.

The instant invention pertains to a semiconductor package that comprises a semiconductor having electrodes on upper and lower faces thereof such that the semiconductor can be electrically connected with a circuit board via the electrode on the upper face. Such a semiconductor package is generally known in the art as shown by Figure 12. However, this known semiconductor package suffers from drawbacks as follows.

First, a wire 4 is used to interconnect the electrode on the upper face of the semiconductor and the circuit board. Using such a wire results in a distance between the electrode on the upper face of the semiconductor and the circuit board being large. This is so because the diameter and other parameters of the wire prevent it from being bent or otherwise shaped so as to minimize a distance between the circuit board and the semiconductor. Such large distance between the electrode and the circuit board can result in a large power loss, and prevents miniaturizing a mounting area around the semiconductor.

Second, when the semiconductor 1 generates a large amount of heat, the circuit board 7 is not sufficient to radiate this heat. Failure to sufficiently radiate heat generated by the semiconductor limits the use and reliability of the semiconductor package.

Applicants have addressed and resolved these drawbacks by providing a unique semiconductor package. Applicants' inventive semiconductor package comprises, with reference to Figures 1 and 2 for example, a semiconductor 1 having electrodes 2 and 3 on an upper face thereof and an electrode on a lower face thereof, a heat radiating plate 10 having a surface to which is joined, via solder or conductive paste, the electrode on the lower face of the first semiconductor, and projecting electrodes 11 joined to the electrodes 2 and 3 and also joined to the heat radiating plate 10. The projecting electrodes 11 can be used to electrically connect the semiconductor 1 to a circuit board.

Thus, projecting electrodes 11 can be used in place of the wire 4 of the conventional semiconductor package as depicted in Figure 12. By using the projecting electrodes 11 in such a manner, the distance between the semiconductor 1 and a circuit board is less than a corresponding distance as shown in Figure 12. This is so because the projecting electrodes 11, unlike the wire 4, can extend perpendicularly to the circuit board. Such decreased distance allows for power loss to be less relative to the power loss associated with the semiconductor package as shown in Figure 12, and also allows for miniaturizing a mounting area around the semiconductor.

Additionally, the heat radiating plate 10 allows for the heat generated by the semiconductor 1 to be radiated to a greater extent than does the circuit board 7 as shown in Figure 12. Accordingly, the semiconductor package as depicted in Figures 1 and 2 is more reliable and exhibits a greater use than does the conventional semiconductor package as depicted in Figure 12.

Claim 27 is believed to be representative of Applicants' inventive semiconductor package.

The Examiner rejected claims 1-4, 6-8, 11 and 13 under 35 U.S.C. 103(a) as being unpatentable over Takahashi et al. in view of Hikita et al. The Examiner rejected claim 5 under 35 U.S.C. 103(a) as being unpatentable over Takahashi et al. and Hikita et al. and further in view of Sakai et al. The Examiner rejected claims 9 and 10 under 35 U.S.C. 103(a) as being unpatentable over Takahashi et al. and Hikita et al. and further in view of Kondoh et al. And, the Examiner rejected claim 12 under 35 U.S.C 103(a) as being unpatentable over Takahashi et al. and Hikita et al. and further in view of Urushima. These rejections are respectfully traversed, and the references relied upon by the Examiner are not applicable with regard to the newly added claims for the following reasons.

In relying on Takahashi et al. to reject claim 1, the Examiner expressed that Takahashi et al. discloses each of the limitations of claim 1 except for pillared or spherical electrodes, i.e. projecting electrodes, joined to the electrodes on the upper face of the semiconductor. It is it respectfully submitted that a further limitation of claim 27 is not taught or suggested by Takahashi et al.

In this regard, claim 27 recites a semiconductor package that comprises a first semiconductor having an upper face electrode on an upper face of the first semiconductor, a **lower face electrode on a lower face** of the first semiconductor, and a heat radiating plate having a surface to which is joined the lower face electrode **via a joining member**.

The lower face electrode as recited in claim 27, or the lower face electrode being connected to a heat radiating plate via a joining member as recited in claim 27, is not taught or suggested by Takahashi et al.

Specifically, while the Examiner has expressed that Takahashi et al. discloses a lower face electrode and that the lower face of the semiconductor 12 is joined to the heat radiating plate 16 by a joining member, the Examiner has failed to specifically identify any component in Figure 2C of Takahashi et al. that corresponds to the claimed "lower face electrode", and also has failed to identify any structure which corresponds to the "joining member".

With regard to Takahashi et al., as expressed in column 1, lines 32-35, it is stated that electrode pads are provided on the upper surfaces of the semiconductor elements 12 as shown in Figure 1B, but Takahashi et al. makes no reference to any similar electrode pads being provided on the lower surface of the semiconductor element 12. Accordingly, with regard to Figure 2C, it follows that electrode pads are provided on the upper surfaces of semiconductor elements 12, but not necessarily that electrode pads are provided on the

lower surfaces of semiconductor elements 12. Accordingly, it is respectfully submitted that Takahashi et al. fails to disclose or suggest a "lower face electrode" as recited in claim 27.

Hikita et al. does not disclose or suggest a semiconductor element having electrodes on both of upper and lower surfaces, and accordingly, even if one would have found it obvious to combine the teachings of Takahashi et al. and Hikita et la., it is respectfully submitted that any combination of Takahashi et al. and Hikita et al. would not result in the invention as recited in claim 27.

With regard to Takahashi et al., it is appreciated that with regard to Figure 1B, the semiconductor element 12 is said to be fixed onto the bed 11a by solder 13. Accordingly, it can arguably be asserted that with regard to Figure 2C, the semiconductor element 12 is mounted to the bed 22a of circuit pattern 22 via solder, whereby this solder can possibly be said to correspond to the claimed "lower face electrode", since it is on a lower face of the semiconductor element 12.

However, if this solder is equated to the "lower face electrode" as recited in claim 27, then the "joining member" as recited in claim 27 would not be disclosed by Takahashi et al. In other words, the solder of Takahashi et al. can possibly be equated to either the "lower face electrode" or the "joining member", as recited in claim 27 but not both. If the solder is equated to a "lower face electrode" then there would be no joining member to join the solder as the lower face electrode to the heat radiating plate as required by claim 27, and if the solder is equated to a "joining member" then there would be no lower face electrode that is joined to the heat radiating plate by the solder as the joining member as required by claim 27.

Hikita et al. does not resolve this deficiency of Takahashi et al., and accordingly, for this additional reason, even if one would have found it obvious to combine Takahashi et al. and Hikita et al., claim 27 would not be obvious over this combination of Takahashi et al. and Hikita et al.

The remaining references relied upon by the Examiner also do not resolve the above deficiencies of Takahashi et al. Accordingly, claims 27-55 are allowable over any combination of references relied upon by the Examiner.

If the Examiner continues to rely on Takahashi et al. in the rejection of the claims, then the Examiner is respectfully requested to specifically explain how the claims are being read on Takahashi et al.

Furthermore assuming arguendo that Takahashi et al. discloses a lower face electrode that is connected to heat radiating plate 16 via a joining member, one having ordinary skill in the art would not have been motivated to combine the teachings of Takahashi et al. and Hikita et al. to arrive at the invention as recited in claim 27. In this regard, because Hikita et al. is not concerned with a semiconductor package including a semiconductor having electrodes provided on upper and lower surfaces thereof, one having ordinary skill in the art would not have been motivated to combine the teachings of Hikita et al. with a semiconductor package having a semiconductor with electrodes on both upper and lower surfaces thereof, i.e. Takahashi et al. Thus, for this further reason claim 27 is allowable.

New claim 55 more specifically recites the joining member as being one of solder and conductive paste in contact with the lower face electrode. In Takahashi et al., even if the solder on the bottom of semiconductor element 12 is said to correspond to an electrode, there is no additional solder or conductive paste in contact with this solder, and accordingly, claim 55 is patentable in its own right.

With regard to originally filed claim 8, and new claim 35 which generally corresponds to originally filed claim 8, it is respectfully noted that the Examiner has failed to specifically address this claim. The subject matter added by originally filed claim 8, and new claim 35, is not taught or suggested by the combination of reference of relied upon by the Examiner.

In this regard, assuming arguendo that one having ordinary skill in the art would have found it obvious to modify Takahashi et al. in view of Hikita et al. for the reasons as expressed by the Examiner, the electrodes provided on the electrode pads on the upper surface of semiconductor element 12 of Takahashi et al. would merely be a bump electrode as disclosed in Figure 7 of Hikita et al., which bump electrode would not nearly extend to the height that pin-like electrode terminals 29 of Takahashi et al. extend. Accordingly, even if Takahashi et al. were modified in view of Hikita et al. as expressed by the Examiner, the resulting combination would **not** result in the leading ends of the projecting electrodes extending to a "uniform height relative to one another" as recited in claim 35. Accordingly, claim 35 is patentable in its own right.

New claim 41 is similar to new claim 35 in that it recites that the projecting electrodes are

> substantially equally spaced relative to one another from said surface of said heat radiating plate

Accordingly, claim 41 is also patentable in its own right, such that claims 41-54 are allowable.

Furthermore, with regard to originally filed claim 2, and new claim 29, were Takahashi et al. modified in view of Hikita et al. as expressed by the Examiner, any bump electrodes provided on the electrode pads on the upper surface of the semiconductor element 12 of Takahashi et al. would be covered in their entirety by the sealing resin of Takahashi et al.

This is contrary to what is required by claim 29, which recites that the sealing resin does not cover the leading ends of the projecting electrodes. Accordingly, claim 29 is patentable in its own right.

Finally, with regard to originally filed claim 4, and new claim 31, neither Takahashi et al. nor Hikita et al. disclose or suggests circuits having "independent polarities". Accordingly, claim 31 is patentable in its own right over a combination of Takahashi et al. and Hikita et al.

In view of the above amendments and remarks, it is respectfully submitted that the present application is in condition for allowance and an early Notice of Allowance is earnestly solicited.

If after reviewing this Amendment, the Examiner believes that any issues remain which must be resolved before the application can be passed to issue, the Examiner is invited to contact the Applicants' undersigned representative by telephone to resolve such issues.

Respectfully submitted,

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Version with Markings to Show Changes Made

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~~SPECIFICATION~~

TITLE OF THE INVENTION

Semiconductor Package And Method For Forming Semiconductor Package

BACKGROUND OF THE INVENTION

The present invention relates to a package for a semiconductor used in electronic equipment and a method for forming the semiconductor package.

A semiconductor is an essential component in forming circuits of electronic equipment and, various forms for mounting ~~the~~ semiconductors have been developed and practiced lately. A form of ~~the~~ a package as shown in Fig. 12 has been employed to facilitate handling and mounting ~~the~~ semiconductors in the prior art.

An example of the aforementioned prior art will be described with reference to the drawing.

Fig. 12 shows a sectional view of a form of a conventional semiconductor package.

A semiconductor 1 has an upper first electrode 2 (upper ~~a~~ electrode) ~~2~~ and an upper second electrode 3 (upper ~~b~~ electrode) ~~3~~ set to one face, and ~~a lower electrode 5 set to the other entire~~ an opposite end in its entirety face. A circuit board 7 has predetermined circuit patterns formed ~~to~~ on both faces which are joined by a through hole conductor (not shown), ~~with~~ thereby forming a single

circuit by the two faces. In some cases, balls 8 essentially consisting of gold, silver, copper, or solder are joined, as connecting bodies for connecting the circuit board 7 to another electric circuit, or to the circuit pattern of another circuit board 7 to facilitate connection of the circuit board 7 to the another electric circuit.

The semiconductor package is formed by joining the semiconductor 1 and the circuit board 7 to one another. First, the lower electrode 5 is joined by solder 6 to the circuit pattern of the circuit board 7. A conductive paste or gold may be used in place of the solder 6 for joining the lower electrode 5 to the circuit pattern.

Meanwhile, the upper first electrode 2 (upper a electrode) and the upper second electrode 3 (upper b electrode) are generally connected to the circuit pattern by wire bonding with use of a gold wire or aluminum wire 4.

In order to protect a circuit forming part primarily consisting of the semiconductor 1, the circuit board 7 at the ~~side of the~~ face to which the semiconductor 1 is mounted is coated with ~~use of~~ an insulating resin 9 in a manner not to deform the joining gold wire or aluminum wire 4. The semiconductor package is formed in this manner ~~with~~ a protection effect and ease of use improved.

The insulating resin 9 is supplied by molding with use of a mold, pouring the molten resin ~~or~~, heating and

melting the resin in the form of powder or particles after placing the resin on an upper face of the semiconductor 1, by or a similar manner, thereby coating the semiconductor entirely, ~~or the like manner~~.

When the semiconductor is heated to a great extent ~~heats by a larger amount~~ in the above-described constitution, the circuit board is not sufficient ~~enough~~ to radiate heat. Even if the circuit board is formed of ceramic exhibiting ~~of a~~ good heat conductivity, and used to radiate heat to a heat radiating plate or the like, emphasis is put on forming the circuit pattern, that is, heat radiation is not ~~less~~ considerable taken into consideration, whereby a radiation loss is easily generated ~~easy to generate~~. Also, even if the gold wire or aluminum wire is utilized to radiate heat, since the gold wire or aluminum wire used for wire bonding is limited in diameter, the wire should be used within a current capacity allowed for its diameter. A plurality of joints must be carried out for ~~to~~ one electrode to cope with a large current as in a power source circuit. Although a distance between electrodes must be secured to ensure safety and reliability in accordance with a current increase, the distance is hard to secure in the case where ~~of~~ the gold wire or aluminum wire is used because the wire is varied in shape at the time of wire bonding, ~~or~~ deformed during subsequent processes ~~afterwards~~, or the like.

SUMMARY OF THE INVENTION

An ~~The~~ object of the present invention is accordingly to resolve ~~remove~~ the above issues and provide a semiconductor

package which is comprised of one or a plurality of semiconductors and can exhibit a superior heat radiation effect with the semiconductor package being of a simple structure and a stable quality, and a method for forming the semiconductor package is also an object of the invention.

In order to accomplish the above objectives the present invention is constituted as will be described below.

In accomplishing these and other aspects, according to a first aspect of the present invention, there is provided a semiconductor package comprising:

a first semiconductor having electrodes formed on both of an upper and a lower face;

a heat radiating plate to which a lower face electrode of the first semiconductor is joined with use of a joining member; and

pillared (columnar) or spherical (i.e. projecting electrodes) electrodes which are joined to the upper face electrodes of the first semiconductor and the heat radiating plate, respectively.

According to a second aspect of the present invention, there is provided a semiconductor package according to the first aspect, further comprising a sealing resin with which the first semiconductor and a face of the heat radiating plate joined to the first semiconductor are covered in a manner to expose a part of leading ends of the pillared or spherical electrodes.

According to a third aspect of the present

invention, there is provided a semiconductor package according to the first or second aspect, further comprising a second semiconductor having electrodes formed ~~to~~ on both of an upper and a lower face, being and of the same kind ~~of~~ as the first semiconductor. A lower face electrode of the second semiconductor ~~being~~ is joined to the heat radiating plate with use of a joining member. The heat radiating plate ~~having~~ has an electric circuit of an equal polarity formed of a single or a combination ~~material~~ one of gold, silver, copper, nickel, and tungsten and set to ceramic, with the first and second semiconductors being joined to the electric circuit of ~~the~~ equal polarity.

According to a fourth aspect of the present invention, there is provided a semiconductor package according to the first or second aspect, further comprising a third semiconductor having electrodes formed ~~to~~ on both of an upper and a lower face, being and of a different kind ~~of~~ relative to the first semiconductor. A lower face electrode of the third semiconductor ~~being~~ is joined to the heat radiating plate with use of a joining member. The heat radiating plate ~~having~~ has an electric circuit of a plurality of polarities ~~independently~~, independent with the circuit being formed of a single or a combination one of ~~material~~ of gold, silver, copper, nickel, and tungsten and set to ceramic, ~~and~~ with the first and third semiconductors of ~~the~~ different kinds being joined respectively to the

plurality of polarities of the electric circuit.

According to a fifth aspect of the present invention, there is provided a semiconductor package according to any one of the first through fourth aspects, wherein the heat radiating plate is constituted of ceramic ~~in a~~ multilayer structure, having a circuit for the semiconductor and the pillared or spherical electrodes, ~~with~~ the circuit ~~being~~ is formed of a single or a combination ~~material~~ of gold, silver, copper, nickel, and tungsten and one of set to a front face ~~thereof, and~~ of the heat radiating plate the heat radiating plate has ~~conductor~~ conductive layers formed of ~~an equal~~ a material to a material of the electrodes ~~on~~ of the front face ~~thereof~~ of the heat radiating plate, and arranged between layers of the ceramic to be connected to the circuit ~~on~~ of the front face, of the heat radiating plate so that heat of the semiconductor is radiated by both the ceramic and the ~~conductor~~ conductive layers.

According to a sixth aspect of the present invention, there is provided a semiconductor package according to the first or second aspect, wherein the heat radiating plate is formed of any one ~~material~~ of copper, a copper alloy, aluminum, and an aluminum alloy, or any one of ~~the~~ these metals subjected to surface treatment.

According to a seventh aspect of the present invention, there is provided a semiconductor package according to any one of the ~~first to second~~ through sixth

aspects, wherein ~~a sealing resin and~~ exposed leading ends of the pillared or spherical electrodes are formed by removing simultaneously part of ~~the~~ a sealing resin and part of the pillared or spherical electrodes after the pillared or spherical electrodes are covered with the sealing resin, thereby exposing the pillared or spherical electrodes to constitute electric connecting parts.

According to an eighth aspect of the present invention, there is provided a semiconductor package according to any one of the first through seventh aspects, wherein the pillared or spherical electrodes have leading ends pressed smoothly to a uniform height.

According to a ninth aspect of the present invention, there is provided a semiconductor package according to any one of the first through eighth aspects, wherein the pillared or spherical electrodes ~~is~~ are formed ~~of~~ to have materials of different hardnesses ~~between~~ constituting an inside thereof and an outside thereof, respectively.

According to a ~~10th~~ tenth aspect of the present invention, there is provided a semiconductor package according to any one of the first through eighth aspects, wherein the pillared or spherical electrodes ~~is~~ are formed ~~of~~ to have materials of different melting temperatures ~~between~~ constituting an inside thereof and an outside thereof, respectively.

According to an ~~11th~~ eleventh aspect of the present

invention, there is provided a semiconductor package according to any one of the first through third aspects, ~~wherein~~ further comprising a fourth semiconductor having electrodes formed ~~to~~ on both of an upper and a lower face relative to and being of a different kind ~~of~~ the first semiconductor. The fourth semiconductor ~~and having a~~ has a lower face electrode of ~~an~~ equal current and voltage characteristics relative to those of the first semiconductor. The lower face electrode of the fourth semiconductor ~~being~~ is joined to the heat radiating plate with use of a joining member, such that the ~~first~~ and fourth semiconductors ~~are~~ is mounted on the heat radiating plate along with the first semiconductor.

According to a ~~12th~~ twelfth aspect of the present invention, there is provided a semiconductor package according to any one of the first through ~~11th~~ eleventh aspects, wherein the heat radiating plate is provided with pits and projections ~~to~~ on a ~~front face of a~~ face opposite to a face joined to the semiconductors.

According to a ~~13th~~ thirteenth aspect of the present invention, there is provided a semiconductor package according to any one of the first through ~~12th~~ twelfth aspects, wherein a plurality of bumps are disposed between the upper face electrodes of the semiconductors and the pillared or spherical electrodes.

According to a ~~14th~~ fourteenth aspect of the present invention, there is provided a method for forming a

semiconductor package, comprising:

joining a lower face electrode of a first semiconductor, which has electrodes formed ~~to~~ on both of an upper and a lower face, to a heat radiating plate with use of a joining member; and

joining pillared (columnar), or spherical electrodes to ~~the~~ upper face electrodes of the first semiconductor and the heat radiating plate, respectively.

According to a ~~15th~~ fifteenth aspect of the present invention, there is provided a method for forming a semiconductor package according to the ~~14th~~ fourteenth aspect, further comprising, after the pillared or spherical electrodes are respectively joined to the upper face electrodes of the first semiconductor and the heat radiating plate, covering the first semiconductor and a face of the heat radiating plate joined to the first semiconductor with a sealing resin in a manner to expose a part of leading ends of the pillared or spherical electrodes.

According to a ~~16th~~ sixteenth aspect of the present invention, there is provided a method for forming a semiconductor package according to the ~~14th~~ fourteenth or ~~15th~~ fifteenth aspect, wherein when the first semiconductor is joined to the heat radiating plate, a lower face electrode of a second semiconductor, of the same kind ~~of~~ as the first semiconductor ~~which has~~ and having electrodes formed ~~to~~ on both of an upper and a lower

face is joined to the heat radiating plate with use of a joining member. ~~and the~~ first and second semiconductors are joined to an electric circuit ~~of an equal~~ polarity of the heat radiating plate, with the electric circuit of ~~the~~ equal polarity being formed of a single or a combination ~~material~~ of gold, silver, copper, nickel, and tungsten, and set to ceramic.

According to a ~~17th~~ aspect of the present invention, there is provided a method for forming a semiconductor package according to the ~~14th~~ or ~~15th~~ aspect, wherein when the first semiconductor is joined to the heat radiating plate, a lower face electrode of a third semiconductor, of a different kind ~~of~~ the first semiconductor ~~which has~~ electrodes formed ~~to~~ both of an upper and a lower face is joined to the heat radiating plate with use of a joining member. ~~and~~ The first and third semiconductors are joined to an electric circuit of a plurality of polarities ~~independently~~ ~~of~~ the heat radiating plate, with the electric circuit being formed of a single or a combination ~~material~~ of gold, silver, copper, nickel, and tungsten, and set to ceramic.

According to an ~~18th~~ aspect of the present invention, there is provided a method for forming a semiconductor package according to any one of the ~~14th~~ through ~~17th~~ aspects, further comprising, before the

semiconductor is joined to the heat radiating plate, forming on a front face of the heat radiating plate constituted of a ceramic ~~in a layer~~ multilayer structure, a circuit for the semiconductors and the pillared or spherical electrodes ~~by~~ from a single or a combination ~~material~~ of gold, silver, copper, nickel, and tungsten, and arranging ~~conductor~~ conductive layers, of ~~an~~ a ~~equal~~ equal material to a material of the electrodes ~~of~~ on the front face between layers of the ceramic to be connected to the circuits ~~of~~ on the front face ~~thereof~~ of the heat radiating plate, so that heat of the semiconductors is radiated by both the ceramic layers and the ~~conductor~~ conductive layers.

According to a ~~19th~~ nineteenth aspect of the present invention, there is provided a method for forming a semiconductor package according to the ~~14th~~ fourteenth or ~~16th~~ sixteenth aspect, wherein, ~~before the semiconductor is joined to the heat radiating plate, forming~~ the heat radiating plate is formed from ~~by~~ any one ~~material~~ of copper, a copper alloy, aluminum, and an aluminum alloy, or any one of ~~the~~ these metals subjected to surface treatment before the semiconductor is joined to the heat radiating plate.

According to a ~~20th~~ twentieth aspect of the present invention, there is provided a method for forming a semiconductor package according to any one of the ~~14th~~ fourteenth through ~~19th~~ nineteenth aspects, further comprising:

after the pillared or spherical electrodes are respectively joined to the upper face electrodes of the

first semiconductor and the heat radiating plate, covering the pillared or spherical electrodes with ~~the~~ a sealing resin; and

thereafter removing part of the sealing resin and part of the pillared or spherical electrodes simultaneously, thereby exposing the pillared or spherical electrodes to constitute electric connecting parts.

According to a ~~21st~~ twenty first aspect of the present invention, there is provided a method for forming a semiconductor package according to any one of the ~~14th~~ fourteenth through ~~20th~~ twentieth aspects, further comprising, after the pillared or spherical electrodes are respectively joined to the upper face electrodes of the first semiconductor and the heat radiating plate, pressing smoothly leading ends of the pillared or spherical electrodes to a uniform height.

According to a ~~22nd~~ twenty second aspect of the present invention, there is provided a method for forming a semiconductor package according to any one of the ~~14th~~ fourteenth through ~~21st~~ twenty first aspects, wherein when the pillared or spherical electrodes are respectively joined to the upper face electrodes of the first semiconductor and the heat radiating plate, the pillared or spherical electrodes ~~are formed~~ are which constitute and of materials of different hardnesses ~~between~~ an inside ~~thereof~~ of the pillared or spherical electrodes respectively ~~and~~ an outside ~~thereof is used~~.

According to a ~~23rd~~ twenty third aspect of the present

invention, there is provided a method for forming a semiconductor package according to any one of the ~~14th~~ fourteenth through ~~21st~~ twenty first aspects, wherein when the pillared or spherical electrodes are respectively joined to the upper face electrodes of the first semiconductor and the heat radiating plate, the pillared or spherical electrodes ~~formed~~ are of materials of different melting temperatures ~~between~~ which constitute an inside ~~thereof~~ and an outside ~~thereof is used~~ of the pillared or spherical electrodes, respectively.

According to a ~~24th~~ twenty fourth aspect of the present invention, there is provided a method for forming a semiconductor package according to any one of the ~~14th~~ fourteenth through ~~16th~~ sixteenth aspects, wherein when the first semiconductor is joined to the heat radiating plate, a lower face electrode of a fourth semiconductor, having electrodes formed ~~on~~ both of an upper and a lower face, thereof being and of a different kind ~~of~~ relative to the first semiconductor, ~~and having~~ with the lower face electrode ~~of an equal~~ having current and voltage characteristics equal to that of the first semiconductor, is joined to the heat radiating plate with use of a joining member, so that the first and fourth semiconductors ~~are~~ is mounted on the heat radiating plate.

According to a ~~25th~~ twenty fifth aspect of the present invention, there is provided a method for forming a semiconductor package according to any one of the ~~14th~~ fourteenth through ~~24th~~ twenty fourth aspects, further comprising providing the heat

radiating plate with pits and projections at a ~~front face of~~ face opposite to the face joined to the semiconductors.

According to a ~~26th~~ twenty sixth aspect of the present invention, there is provided a method for forming a semiconductor package according to any one of the ~~14th~~ Fourteenth through ~~25th~~ twenty fifth aspects, further comprising forming a plurality of bumps on the upper face electrodes of the semiconductors,

wherein when the pillared or spherical electrodes are joined to the upper face electrodes of the semiconductors, the pillared or spherical electrodes are joined to the upper face electrodes of the semiconductors via the plurality of bumps.

BRIEF DESCRIPTION OF THE DRAWINGS

These and other aspects and features of the present invention will become clear from the following description taken in conjunction with the preferred embodiments thereof with reference to the accompanying drawings, in which:

Fig. 1 is a plan view of a semiconductor package according to a first embodiment of the present invention;

Fig. 2 is a sectional view of the semiconductor package of the first embodiment of the present invention taken along a line A-A of Fig. 1;

Fig. 3 is a sectional view of a semiconductor package according to a second embodiment of the present

invention;

Fig. 4 is a plan view of a semiconductor package according to a third embodiment of the present invention;

Fig. 5 is a sectional view of the semiconductor package of the third embodiment of the present invention taken along a line B-B of Fig. 4;

Fig. 6 is a sectional view of a semiconductor package according to a fourth embodiment of the present invention assumed to be cut along a line B-B' of Fig. 4;

Figs. 7A and 7B are sectional views of a semiconductor package according to a sixth embodiment of the present invention;

Figs. 8A and 8B are sectional views of a semiconductor package according to a seventh embodiment of the present invention;

Figs. 9A, 9B, and 9C are sectional views of a semiconductor package according to an eighth embodiment of the present invention;

Fig. 10 is a sectional view of a semiconductor package according to a ninth embodiment of the present invention;

Figs. 11A and 11B are a plan view and a sectional view of a semiconductor package according to a ~~10th~~ tenth embodiment of the present invention;

Fig. 12 is a sectional view of a semiconductor

package of the prior art;

Fig. 13 is a plan view of the semiconductor package of the third embodiment of the present invention when electric circuits of equal polarity are formed on the entire surface of a ceramic radiating plate;

Fig. 14 is a sectional view showing a state of joining a circuit board and a semiconductor element with use of the semiconductor package of one example of the eighth embodiment of the present invention;

Fig. 15 is a sectional view of a state of joining a circuit board and a semiconductor element with use of the semiconductor package of another example of the eighth embodiment of the present invention; and

Figs. 16, 17, and 18 are sectional views of semiconductor packages according to other examples of the eighth embodiment of the present invention.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

Before the description of the present invention proceeds, it is to be noted that like parts are designated by like reference numerals throughout the accompanying drawings.

Semiconductor packages and methods for forming the semiconductor packages according to embodiments of the present invention will be discussed in detail below on the basis of drawings.

(FIRST EMBODIMENT)

Fig. 1 is a plan view of a semiconductor package according to a first embodiment of the present invention, and Fig. 2 is a sectional view of the semiconductor package.

In the semiconductor package according to the first embodiment of the present invention, ~~the~~ a lower face electrode of a semiconductor 1, ~~has~~ having electrodes formed ~~to~~ on both upper and lower faces, ~~and the lower face electrode of the semiconductor 1~~ is joined to a heat radiating plate 10 with use of ~~a~~ solder, ~~and the~~ upper face electrodes 2 and 3 of the semiconductor 1, and the radiating plate 10, are joined to pillared (columnar) or spherical (i.e. projecting electrodes) electrodes 11.

The ~~metallic~~ heat radiating plate 10 is formed of any one of copper, a copper alloy, aluminum, and an aluminum alloy. The metallic radiating plate 10 and ~~the~~ a/the ~~lower electrode~~ lower face electrode of the semiconductor 1 ~~having the electrodes to the upper and lower both faces~~ on both are joined ~~with~~ to each other by ~~the~~ solder. A thickness of a layer formed of the solder is made as small as possible, so that its heat conduction efficiency is improved. Other examples of ~~the~~ a joining member are conductive paste, gold, or the like. When the joining member is solder, heat conductance, joining properties (~~easiness~~ ease of joining) ~~to~~ of the semiconductor, and heat resistance may be improved. When the embodiment is applied to drivers of industrial motors

such as AC servo motors, and there is caused any lock of the rotation of the motor to generate heat of about 120°C to which the joining member is subjected, such a joining member is preferably formed of solder. When the joining member is of gold, the heat conduction properties become high and the electrical resistance becomes lower.

The pillared or spherical electrodes 11 formed of a metal essentially consisting of any one of gold, silver, copper, and aluminum are joined to the upper first electrode (upper a electrode) 2 and the upper second electrode (upper b electrode) 3 of the semiconductor 1, and to the metallic radiating plate 10 with use of ultrasonic oscillation, solder, or conductive paste. The conductive paste is a mixture of a metallic powder such as gold, silver, or the like and generally an epoxy resin or silicone resin having thermosetting properties and insulating properties, thereby exhibiting electric conductive and adhesive properties.

Leading end parts of the pillared or spherical electrodes 11 at the side not to be joined to the semiconductor 1 and the metallic radiating plate 10 are used for joining to a circuit board after the semiconductor package is completed. For this purpose, it is necessary to form the pillared or spherical electrodes 11 without a step, in other words, at an approximately equal height.

Mixed-mounting of semiconductors 1 of different

kinds can be carried out on the metallic radiating plate 10 if the semiconductors have equal current and voltage characteristics ~~related~~ relative to the lower face electrodes.

In the above constitution, the lower face electrode of the semiconductor 1 is joined to the radiating plate 10 with use of the solder, while the upper face electrodes ~~(upper face electrodes)~~ 2 and 3 of the semiconductor 1, and the radiating plate 10, are joined to the pillared or spherical electrodes 11. When ~~the~~ a radiating plate 10 of ~~the~~ metal is used, the semiconductor 1 is always joined directly only via the solder to the metallic radiating plate 10, so that ~~the~~ heat of the semiconductor 1 is considerably quickly transmitted to the metallic radiating plate 10, spread throughout entirety ~~in the whole~~ of the radiating plate 10 and radiated from a surface of the radiating plate 10. A temperature rise of the semiconductor 1 is accordingly prevented. Moreover, the metallic radiating plate 10 is utilizable as a conductor for the lower face electrode if a connecting terminal is joined to the radiating plate 10.

(SECOND EMBODIMENT)

Fig. 3 is a sectional view of a semiconductor package according to a second embodiment of the present invention which uses a sealing resin 12 having insulating property ~~ty~~.

The semiconductor package in the second embodiment

of the present invention is formed by covering the semiconductor package of the first embodiment with the sealing resin 12 in a manner to partly expose the pillared or spherical electrodes 11.

More specifically, after joining the pillared or spherical electrodes 11 of the first embodiment, the semiconductor 1 is covered with the sealing resin 12 ~~with~~ by use of a mold or jig so that end parts of the pillared or spherical electrodes 11 at ~~the~~ a side to be joined to the circuit board project from the sealing resin 12, e.g., by approximately 50-200μm, thereby forming projecting parts 13.

When the mold is to be used, the semiconductor package of the first embodiment is arranged beforehand within a cavity of the mold. ~~The~~ A molten sealing resin 12 is injected into the cavity generally by injection molding, then cooled and hardened. When the jig is to be used, on the other hand, the metallic radiating plate 10 is surrounded ~~in the periphery~~ peripherally by a material not to be joined to the sealing resin 12, and then ~~the~~ molten sealing resin 12 is poured ~~therein~~ between the metallic radiating plate and the material, cooled and hardened. Alternatively, a specified amount of ~~the~~ powder or particle sealing resin 12 is ~~put in~~ provided along the periphery of the radiating plate 10, heated, melted, cooled and hardened.

In the above-described arrangement, after the lower face electrode of the semiconductor 1 ~~having the electrodes to the upper and lower faces~~ on its is joined to the

radiating plate 10 with use of the solder and, the upper face electrodes 2 and 3 of the semiconductor 1, and the radiating plate 10, are joined to the pillared or spherical electrodes 11, the semiconductor 1 is covered with the sealing resin 12 to expose the projecting parts 13 as part of the pillared or spherical electrodes 11. Since the semiconductor 1 is covered with the sealing resin 12, except for the projecting parts ~~leading end~~ 13 of the pillared or spherical electrodes 11, each component is protected from deformation, damage, moisture, dust, or the like and the semiconductor package after completion ~~completed~~ becomes easy to handle.

(THIRD EMBODIMENT)

Figs. 4 and 5 are a plan view and a sectional view of a semiconductor package according to a third embodiment of the present invention which uses a ceramic radiating plate 14 having insulating properties ~~property~~.

In Figs. 4 and 5, an electric ~~electrode~~ circuit ~~15~~ (15A, 15B) for joining ~~the~~ a lower electrode of the semiconductor ~~1~~ (1A, 1B) is formed ~~to~~ on an upper face of the ceramic radiating plate 14 with use of gold, silver, copper, nickel, tungsten, or the like.

In the case where only one semiconductor ~~1 of the same kind~~ is to be mounted, where a plurality of semiconductors ~~1~~ of the same kind are to be mounted, or where a plurality of semiconductors 1A, 1B of different kinds with equal current and voltage

characteristics at ~~the side of the lower electrodes~~ a side of the lower face electrodes are to be mounted, ~~the~~ an electrode circuit 15 ~~(15A or 15B)~~ of an equal polarity is formed of the aforementioned material on the entire surface of the ceramic radiating plate 14 as shown in Fig. 13.

On the other hand, in the case where a plurality of semiconductors 1A and 1B of different kinds and different current and voltage characteristics at the side of the lower face electrodes are to be mounted, ~~electrode~~ electric circuits 15A and 15B of a plurality of different polarities independently of each other are formed for the lower face electrodes of respective semiconductors 1A and 1B, on which are to be set the pillared or spherical electrodes 11 ~~for the lower electrodes~~, as shown in Fig. 4.

Any of the semiconductors ~~1, 1A, and 1B~~ is mounted by soldering onto the ~~formed~~ electric circuit 15, 15A, 15B, respectively. Thereafter, the pillared or spherical electrodes 11 are joined to ~~the~~ respective ones of the semiconductors ~~1, 1A, 1B~~ and the ~~electrode~~ electric circuits 15, 15A, 15B with use of any one of ultrasonic oscillation, solder, and conductive paste.

In forming the ~~electrode~~ electric circuit 15 of a conductive paste, a resin component in the conductive paste is preferably burnt by baking at 600-1600°C to effectuate an intermetallic bond, so that the heat conduction efficiency is improved through firm joining of the circuit 15 with the ceramic radiating plate 14.

Generally, when ~~the~~ current and voltage characteristics are different between lower face electrodes of semiconductors 1A and 1B of different kinds to be mounted on the same radiating plate 14, the mounting is impossible if the radiating plate is metallic. However, in ~~the~~ an arrangement ~~of the third embodiment,~~ where the electric circuit 15 of the same polarity, or electric circuits 15A and 15B of a plurality of polarities are formed of a single one of or a combination ~~material~~ of gold, silver, copper, nickel, or tungsten ~~to~~ on the entire face or part of the face of the ceramic radiating plate 14, while the radiating plate 14 and ~~the~~ the semiconductors ~~1, or 1A and 1B~~ are joined ~~and also~~ the radiating plate 14 and the pillared or spherical electrodes 11 are also joined. Since the plurality of polarities are provided independently of each other on the radiating plate 14 with utilization of insulating, heat conductive, and radiation properties of the ceramic radiating plate 14, the semiconductors can be independent and mounted on an equal face. At the same time, when ~~the~~ a semiconductor is covered with the sealing resin 12 in the application of the earlier second embodiment, since the radiating plate 14 itself is an insulator, electrically active parts except the leading end parts 13 of the pillared or spherical electrodes 11 to be connected to ~~the~~ a circuit board are prevented from being exposed, ~~therefore being improved in~~ thereby improving safety and reliability.

Moreover, a thin wiring is eliminated and an allowable current can be made large when the ~~electric~~ circuit 15 of an equal polarity is formed. An area of a metallic wiring conducting heat well is increased, whereby heat radiation properties can be improved.

(FOURTH EMBODIMENT)

A semiconductor package according to a fourth embodiment of the present invention will be described with reference to Fig. 6. Fig. 6 is a sectional view of a ~~multilayer of~~ ceramic radiating plate ~~of~~ 40.

The semiconductor package ~~in~~ of the fourth embodiment has a radiating plate 40 formed of ceramic layers 14a and 14b ~~in a layered structure~~. ~~The~~ A semiconductor 1 and electrodes for pillared or spherical electrodes are formed of a single one of or a combination ~~material~~ of gold, silver, copper, nickel, and tungsten ~~to~~ on a front face of the radiating plate 40, and ~~conductor~~ conductive layers to be connected to the electrodes of the front face are formed of ~~an equal~~ material equal to a material of the electrodes of the front face, between the ceramic layers 14a and 14b of the radiating plate 40. Heat of the semiconductor 1 is accordingly radiated by both the ceramic layers 14a, 14b, and the ~~conductor~~ conductive layers.

A method for forming the ~~ceramic of the radiating plate 40 in many layers~~ layers 14a and 14b is not different from generally ~~used ones~~ performed methods. For instance, in the case where the radiating plate

40 is constituted of an upper ceramic plate 14a and a lower ceramic plate 14b, holes 16 are formed in the upper ceramic plate 14a and electric circuit(s) 15C are formed on a front face of the upper ceramic plate 14a. Moreover, a material equal to a material of the electric circuit(s) 15C is filled into the holes 16, thereby forming conductive portions 15D. In the meantime, electric circuits of a necessary area are formed as internal conductors 17 on a front face of the lower ceramic plate 14b. Thereafter, the upper ceramic plate 14a and lower ceramic plate 14b are united while the conductive portions 15D of the upper ceramic plate 14a are electrically joined with the internal conductors 17 of the lower ceramic plate 14b, as shown in Fig. 6. The ceramic plate 14a and ceramic plate 14b are united via use of an adhesion force generated as a result of drying and baking a conductive paste used for forming the electric circuit(s) 15C, conductive portions 15D, and the internal conductors 17, or via use of another adhesive so that the ceramic plate 14a and ceramic plate 14b are joined to each other. Another method uses a ceramic green sheet, in which the above upper and lower ceramic plates 14a and 14b are replaced with ceramic green sheets. After the same process as above, the ceramic green sheets and conductive paste are simultaneously baked and united at 600-1600°C. The semiconductor 1 and pillared or spherical electrodes 11 are mounted to the thus-formed

ceramic radiating plate 40, whereby the semiconductor package is completed as indicated in Fig. 6.

In this case, the heat generated at the semiconductor 1 is directly transmitted to the joined electrode circuits 15C and to the internal conductors 17 via the conductor layers 15D inside the holes 16 further to the ceramic plate 14b. The heat is radiated from a lower surface of the lower ceramic plate 14b. Although the radiating plate 40 in the figure is constituted of two ceramic plates 14a and 14b, the ceramic plates can be overlapped in many layers by repeating the same process.

Normally, the transmission of heat is carried out not only via the conductor layers 15D in the holes 16, but through every joined part.

In the arrangement, the radiating plate 40 is constructed in a layered structure of ceramic, with having the semiconductor 1 and the electrodes for pillared or spherical electrodes 11 formed of a single or a combination of material of gold, silver, copper, nickel, and tungsten to the front face and having conductor layers 15C, 15D, and 17, formed of the same material as the material of the electrodes of the front face, between the ceramic layers to be connected with the electrodes of the front face, so that the heat is radiated both from the ceramic radiating plate 40 and the conductor layers 15C, 15D, and 17. More

specifically, a heat conduction performance of the metal is utilized in order to improve more heat radiation efficiency of the ceramic of the radiating plate 40. In addition, the conductive portions conductor layers 15D and internal conductors 17 are set as a heat-transmitting metallic layer inside the ceramic of the radiating plate 40 to be connected to the electronic electric circuit(s) 15C of the front face of the radiating plate 40 connected with the semiconductor 1 in order to transmit the heat generated at the semiconductor 1 as fast as possible to the entirety whole of the radiating plate 40. The heat can thus be transmitted from the electronic electric circuit(s) 15C through the conductive portions conductor layers 15D and the internal conductors 17 to the lower ceramic plate 14b. A heat diffusion efficiency can be improved, and the heat radiation efficiency can also be made improved further better.

(FIFTH EMBODIMENT)

In a semiconductor package according to a fifth embodiment of the present invention, the radiating plate is formed of any one single material of copper, a copper alloy, aluminum, and an aluminum alloy, or the one metal thereof after subjected to surface treatment. Since the copper, a copper alloy, aluminum, or an aluminum alloy has a good processability to allow various working methods of cutting, casting, and the like, a large degree of freedom in shape is effectuated and a use range is enlarged in combination with the surface

treatment.

As above, when the radiating plate is formed of any one ~~material~~ of copper, a copper alloy, aluminum, and an aluminum alloy or the one metal ~~thereof~~ after subjected to the surface treatment, if one semiconductor 1 is to be mounted, or a plurality of semiconductors 1 including lower face electrodes of ~~an~~ equal current and voltage characteristics are to be mounted, the radiating plate itself may be a conductor. Since the above materials transmits heat and electricity well, diffuses heat fast, and is easy to solder to other ~~among~~ metals, the heat of the semiconductor 1 can be radiated more effectively.

(SIXTH EMBODIMENT)

A semiconductor package of a sixth embodiment of the present invention will be described with reference to Figs. 7A and 7B.

The semiconductor package of the sixth embodiment of the present invention is obtained by covering pillared or spherical electrodes 11 with the sealing resin 12 as shown in Fig. 7A, and then simultaneously removing part of the sealing resin 12 and part of the pillared or spherical electrodes 11 to expose electrode parts of the pillared or spherical electrodes 11, thereby forming connecting parts as shown in Fig. 7B.

More specifically, in Fig. 7A, a semiconductor 1

and the pillared or spherical electrodes 11 mounted on an ~~electrode~~ electric circuit of ~~the~~ a metallic radiating plate 10, or ceramic radiating plate 14, are covered with the sealing resin 12 with use of a mold or a jig as described in the second embodiment. The sealing resin 12 is applied ~~by~~ in an amount at least covering leading end parts of the pillared or spherical electrodes 11, preferably, an amount whereby a margin is provided ~~to~~ at the leading end parts as indicated in Fig. 7A. Thereafter, in Fig. 7B, a part 18, that is, an upper part of the pillared or spherical electrodes 11, and part of the sealing resin 12 formed in Fig. 7A is removed, whereby a smooth face 19 is formed and end faces of the pillared or spherical electrodes 11 are exposed.

The part 18 is removed by cutting by means of a rotating or reciprocating cutting tool, or rotating an abrasive paper.

The removal is carried out on the basis of a lower face of the metallic radiating plate 10 or ceramic radiating plate 14, whereby a total height is uniformed without the need of carefully taking the amount of the sealing resin 12 ~~into account~~ in account.

According to this constitution, part of the sealing resin 12 and part of the pillared or spherical electrodes 11 are removed at the same time after the pillared or spherical electrodes 11 are covered with the

sealing resin 12, thereby exposing the electrode parts of the pillared or spherical electrodes 11 to form the connecting parts. Electrodes are accurately uniformed in height. In other words, although it is considerably difficult to make uniform a plurality of electrodes 11 in height when the pillared or spherical electrodes 11 are set on the ~~electrode~~ electric circuit of the semiconductors 1 and the metallic radiating plate 10 or ceramic radiating plate 14, all the electrodes 11 can be made uniform in height by removing part of all electrodes 11 together with part of the sealing resin 12, so that an accuracy necessary for mounting can be fully satisfied.

(SEVENTH EMBODIMENT)

A semiconductor package according to a seventh embodiment of the present invention will be discussed with reference to Figs. 8A and 8B. The semiconductor package of the seventh embodiment of the present invention has pillared or spherical electrodes 11 joined to the semiconductors 1 and a metallic radiating plate 10 or ceramic radiating plate 14, or sealed with the sealing resin 12, and pressed smoothly thereafter.

The pillared or spherical electrodes 11 joined to the semiconductors 1 and the metallic radiating plate 10 or ceramic radiating plate 14 are not always constant in height because of working errors of individual parts to be joined to each other, and processing errors at the time of joining

the parts. However, the pillared or spherical electrodes 11 are preferably uniform in height as much as possible when to be mounted to a circuit board. Therefore, leading end parts of the pillared or spherical electrodes 11 are pressed to be deformed by a smoothing plate 20 having a smooth face, thereby providing a uniform ~~uniforming the~~ height. Fig. 8A is a diagram of a state in which the electrodes are pressed in the absence of the sealing resin 12, whereby a pressure of the pressing is directly transmitted to joined parts via ~~with~~ the semiconductors 1 because of no sealing resin 12. As such, the pressing force should be determined with breakage ~~a break~~ of the semiconductors 1 being taken into consideration.

In Fig. 8B, the pillared or spherical electrodes 11 are covered with the sealing resin 12 in a manner to expose leading end parts of the electrodes 11 by performance ~~with use~~ of the method in the above-described second embodiment or the like. The pillared or spherical electrodes 11 are pressed by the smoothing plate 20 and deformed at the exposed parts, thereby being made uniformed in height. In this case, a large pressing force is required because the pillared or spherical electrodes 11 include only a small part that can be deformed. However, because the pressing force is supported by the sealing resin 12 and dispersed ~~scattered~~, the pressing force is prevented from being directly transmitted to the semiconductors 1. The semiconductors 1 are accordingly less damaged in

comparison with the process depicted by Fig. 8A. An allowance for a set value of the pressing force can be made large as compared with Fig. 8A, and workability is improved.

According to the above construction, the smooth pressing is conducted after the pillared or spherical electrodes 11 are joined to the semiconductors 1 and the metallic radiating plate 10 or ceramic radiating plate 14, or sealed with the sealing resin 12. The constitution of the embodiment can exhibit the same effects as the sixth embodiment. The pillared or spherical electrodes 11 can be easily made uniform in height by deforming the electrodes 11 through pressing with use of a jig or a mold having a smooth face.

(EIGHTH EMBODIMENT)

A semiconductor package according to an eighth embodiment of the present invention will be described with reference to Figs. 9A, 9B, and 9C, which are sectional views ~~of a pillared electrode 11~~ by way of example of the pillared or spherical electrode 11 of the eighth embodiment of the present invention.

In the eighth embodiment, the pillared electrode 11 is formed of a double structure of different materials. A material constituting an inside and a material constituting an outside are different in hardness.

The pillared electrode 11 in a first example of

the eighth embodiment is in the double structure as shown in Fig. 9A, having a hard inside and a soft outside, or as shown in Figs. 16-18, having the outside formed of a material of a lower melting temperature than the inside. More specifically, Fig. 9A shows the pillared electrode 11 in section, which is formed of an inner member 21 and an outer member 22. The inner member 21 is obtained by cutting a wire or bar stock of copper or a copper alloy to a constant size and finishing a surface smoothly by barrel finishing or the like. The outer member 22 is obtained by plating a material softer than copper, i.e., solder, tin, an alloy of tin and bismuth, or an alloy of tin and lead, to a front face of the inner member 21. A plating thickness of the outer member 22 is, e.g., approximately 20-100μm. When the electrode is pressed in an arrow direction in Fig. 9B at the time of being joined to a substrate, upper and lower soft plated parts of the outer member 22 are deformed as illustrated in Figs. 9B and 14, whereas a hard part of the inner member 21 is not deformed. The entirety of the pillared electrode 11 is prevented from being largely deformed and maintains its shape. In Fig. 14, 42 is a base material and 41 is a copper electrode, which constitute a circuit board 5. Metal diffusion is brought about at a part where the outer member 22 and the copper electrode 41 are in contact with each other, and a part where the outer member 22 and the

aluminum electrode 2 or 3 are in contact with each other. In the constitution of the electrode, a height of the electrode can be determined accurately and a high rigidity can be secured. The plating thickness of the outer member 22 is set to be not smaller than 20μm because this is a minimum value (minimum value from experiments) whereat the plated part is started to be deformed, and a minimum value necessary for absorbing the height variation. The plating thickness of not larger than 100μm of the outer member 22 is set because the value is generally considered as a maximum plating thickness.

Figs. 16-18 show the pillared electrodes 11 in section, each of which is formed of an inner member 21A and an outer member 22B. The inner member 21A is obtained by cutting a wire or bar stock of copper (melting point ~~(melting temperature)~~ of 1084.5°C), aluminum (melting point of 660.4°C), or gold (melting point of 1064.43°C) to a constant size and finishing a surface smoothly by barrel finishing or the like. The outer member 22B is obtained by plating solder (melting point of 180-300°C) such as Sn-Ag-Cu-based, Sn-Cu-based, Sn-Au-based, Sn-Bi-based, or Sn-Pb-based solder, as a material having a melting point lower than that of the inner member 21A, to a front face of the inner member 21A. Because of the solder of the outer member 22B, the joining strength can be ~~more~~ further improved. Even in

this case, similar to Fig. 9A, when the electrode is pressed in the arrow direction in Fig. 9B at the time of ~~joining~~ being joined to ~~the~~ a substrate, ~~an~~ upper and ~~a~~ lower plated parts of the outer member 22B are deformed ~~as~~ similar to that as shown in Figs. 9B and 14, whereas the inner member 21A is not deformed. The ~~whole~~ entirety of the pillared electrode 11 is prevented from being largely deformed and maintains its shape. A dotted line in Fig. 18 shows an electrode of a circuit board.

~~In the meantime~~ Alternatively, in a second example of the eighth embodiment, materials ~~are switched between~~ of the inner member 21 and outer member 22 are switched, that is, the inner member 21 is formed of a wire or rod stock softer than copper, namely, any one of tin, a tin-bismuth alloy, and a tin-lead alloy, which is cut to a constant size and finished smoothly at a front face by barrel finishing or ~~the~~ a like manner. Then, a plated layer of a material harder than the material of the inner member 21, i.e., copper or a copper alloy is formed as the outer member 22 ~~at~~ on ~~the~~ a surface of the inner member 21 ~~in~~ at a thickness of approximately 3-50μm by plating performing a operation. The outer member 22 is prevented from being broken when pressured in an arrow direction of Fig. 9C and, eventually deformed as shown in Figs. 9C and 15. 42 and 41 in Fig. 15 are respectively a base material and a copper electrode which constitute ~~the~~ a circuit board 5. Metal diffusion is brought ~~about to~~ at a contact part between ~~the~~ outer member 22 and the

copper electrode 41, and a contact part between the outer member 22 and the aluminum electrode 2 or 3. According to the constitution, an irregularity in height of the circuit board can be absorbed, and also a uniform pressure is applied to electrodes through the deformation, even when a plurality of electrodes are pressed at one time at the joining time. Different from the foregoing example, the plating thickness of the outer member 22 is set to be not smaller than 3μm, because the inner member 21 is deformed, thereby eliminating the need of deforming the outer member 22. The metal diffusion can be generated good by having the thickness not smaller than 3μm without breaking the outer member. At the same time, the thickness of not larger than 50μm is set because the value approximately half of the plating thickness 100μm of the outer member 22 is considered appropriate.

When the pillared electrode 11 is constituted as in the above first example or second example, the electrode is hard to deform during the joining or the like, whereas the electrode is easy to deform when a height adjustment is required. Excessive pressing is thus not required to adjust the height by the smoothing plate 20 with the application of the seventh embodiment, so that the damage to the semiconductors 1 is eliminated. Furthermore, the work by the smoothing plate 20 is eliminated and the electrode can

be deformed with a small amount of pressing when mounted to the circuit board. The height can be adjusted with an error at the side of the circuit board being absorbed.

To any deformation of the pillared electrodes 11 of the first example and second example, the height adjustment can be by approximately 5-30μm.

As described hereinabove, according to the first example of the eighth embodiment, the pillared or spherical electrode 11 is in the double structure of the soft inside and hard outside, or in the double structure having the outside formed of the material of a lower melting temperature than the inside. In the pillared or spherical electrodes 11 comprised of the inside of copper or copper alloy and the outside of a soft material of any of tin, tin-bismuth alloy, and tin-lead alloy, the soft outer member 22 is deformed at the time of joining to the circuit board, whereas the inner member 21 is supported by the hard copper or copper alloy. The pillared or spherical electrodes 11 show no great deformation as a whole, with a smoothness secured at the leading end parts thereof.

The smoothness can be secured by adjusting the height through smoothly pressing and deforming the electrodes in a heightwise direction, thereby coping with a height irregularity of the electrodes at the side of the circuit board when the electrodes are mounted, as a

semiconductor package, to the circuit board. In other words, ~~absorbing~~ the height irregularity of the electrodes is absorbed on the circuit board.

According to the second example of the eighth embodiment, the pillared or spherical electrode 11 is ~~in the~~ of a double structure ~~of the~~ having a soft inside and hard outside, or ~~in the~~ of a double structure having the outside of the material of a higher melting temperature than that of the material of the inside. The same effect as in the first example can be obtained even by switching with each other the materials ~~between~~ of the inside and the outside of the pillared or spherical electrode 11.

(NINTH EMBODIMENT)

A semiconductor package according to a ninth embodiment of the present invention will be described with reference to Fig. 10. In the ninth embodiment of the present invention, pits and projections are formed ~~to~~ on a ~~front face of an opposite~~ face of the radiating plate that is opposite to the face joined to the semiconductor, so as to increase ~~the~~ surface ~~are~~ area thereof, resulting in improving ~~the~~ heat radiation effect.

In any ~~radiating plate~~ of the metallic radiating plate 10 and ~~the~~ ceramic radiating plates 14, 40, pits and projections 23 are formed ~~to the front face of the~~ on a face opposite (lower face in Fig. 10) ~~to~~ the face (upper face in Fig. 10) where ~~the~~ pillared or spherical electrodes 11 are

mounted to the semiconductors 1, 1A, 1B. Because of the presence of the pits and projections 23 ~~at the front~~ on this face, a surface area is increased and a contact area with the air is increased, so that a heat radiation effect is improved. That is, the instantaneously generated heat of the semiconductors 1, 1A, 1B is absorbed by a part of a large volume density without the pits and projections 23 (namely, the face of the radiating plate where the semiconductors are mounted). Then, the heat is conducted and transmitted to the pits and projections 23 and radiated from the surfaces of the pits and projections 23. Although a sectional shape of the pits and projections 23 is illustrated to be nearly triangular in Fig. 10, the shape is not limited particularly to a triangle and can be ~~rectangle~~ rectangular or a corrugated form, or other forms.

When the pits and projections 23 are formed on ~~to~~ the ~~front face of the~~ face opposite ~~to~~ the face of the radiating plate 10, 14, 40 where the semiconductors 1, 1A, 1B are joined ~~in the construction~~, the surface area of the radiating plate 10, 14, 40 is increased, so that the heat radiation effect can be improved. Since the contact area with the air is increased, an amount of heat of the radiating plate 10, 14, 40 to be radiated into the air is increased, thereby promoting the heat radiation effect.

(TENTH EMBODIMENT)

A semiconductor package according to a ~~10th~~ tenth embodiment of the present invention will be described with reference to Figs. 11A and 11B.

In the ~~10th~~ tenth embodiment of the present invention, a plurality of bumps 24 are formed ~~to~~ on each of ~~the~~ an upper face first electrode 2 (upper a electrode) and ~~the~~ upper face second electrode 3 (upper b electrode) of ~~the~~ semiconductors 1, 1A, 1B (represented by the semiconductor 1 in the description below ~~and the drawings~~), and then, pillared or spherical electrodes 11 are joined ~~then~~ to the plurality of bumps 24. The bumps 24 ~~is~~ are not limited to gold, but may be formed of copper or aluminum. In the case of gold bumps 24, ~~the~~ height stability can be easily ensured. In the case of copper bumps 24, ~~the~~ electrical resistance and ~~the~~ cost can be decreased. In the case of aluminum bumps 24, ~~the~~ processability can be improved.

~~The~~ A plurality of gold bumps 24 ~~of gold~~ are formed ~~to~~ on the upper face first electrode 2 (upper a electrode) ~~of~~ and the upper face second electrode 3 (upper b electrode) ~~of~~ of the semiconductor 1 by a bump formation method using general ultrasonic oscillation. The bumps 24 are preferably formed to be scattered as much as possible ~~inside~~ on the upper face first electrode 2 (upper a electrode) ~~of~~ and the upper face second electrode 3 (upper b electrode) ~~of~~ and in a range not larger than a bottom area of the pillared or spherical electrode 11. If the bumps 24 are formed in an unbalanced state and

concentrated to one side, the pillared or spherical electrode 11 is sometimes inclined ~~at the mount time~~ during mounting of the pillared or spherical electrode 11, or a connection area of the pillared or spherical electrode 11 is apt to be reduced, leading to a connection failure.

A sectional shape of ~~the~~ each bump 24 is not specified. A variation of approximately 10μm in height of the bumps 24 generated when formed is allowed because the bumps are pressed and crushed when the pillared or spherical electrode 11 is mounted. However, for enhancing an effect in height adjustment when the pillared or spherical electrodes 11 are mounted, the bumps are preferably formed as high as possible and no particular problem is brought about when the height is 50μm or more.

According to the above construction, after the plurality of bumps 24 are formed ~~to~~ on each of the upper face first electrode 2 (upper a electrode) and the upper face second electrode 3 (upper b electrode) of the semiconductor 1, the pillared or spherical electrodes 11 are joined to the bumps 24. As compared with the case where large electrodes, i.e., pillared or spherical electrodes 11 are directly joined to the upper face first electrode 2 (upper a electrode) and the upper face second electrode 3 (upper b electrode) of the semiconductor 1, the semiconductor 1 is less damaged when the semiconductor 1 has ~~the~~ small gold bumps 24 formed

~~through~~ via ultrasonic oscillation. When the pillared or spherical electrodes 11 are mounted on the bumps 24 ~~through~~ via ultrasonic oscillation, the bumps 24 are deformed thereby ~~easing~~ lessening a load applied to the semiconductor 1 and adjusting the height of the bumps, ~~The~~ Each gold bump 24 has ~~a~~ good solderability, enabling its joining to the pillared or spherical electrodes 11 by solder.

In each of the above-described embodiments, the lower face electrode of the semiconductor 1, 1A, 1B ~~having the electrodes to both of the upper and lower faces~~ is joined with use of the solder to the radiating plate 10, 14, 40, and moreover the pillared or spherical electrodes 11 are joined to the upper electrodes of the semiconductor and the radiating plate. The semiconductor package is ~~a~~ high reliability can be consequently formed easily and stably. More specifically, the electrode ~~at~~ on one face of each semiconductor 1, 1A, 1B, ~~which has electrodes formed to both faces~~ is directly joined to the radiating plate 10, 14, 40, so that ~~the~~ heat of the semiconductor 1, 1A, 1B can be quickly absorbed and diffused, with ~~the~~ a heat radiation effect improved. At the same time, since the pillared or spherical electrodes 11 thicker than a wire used in wire bonding, and of a larger current capacity than the wire, are employed for the connection, the pillared or spherical electrodes 11 can be utilized as connecting terminals ~~to the~~ for a circuit board.

In the case of the insulating ceramic radiating plate 14, 40, having an insulating function, semiconductors 1A and 1B of different functions can be mounted simultaneously.

The present invention is not limited to the foregoing embodiments and can be executed in other various modes.

For example, each of the above embodiments is primarily related to the case where one semiconductor 1 is mounted on the metallic or ceramic radiating plate 10, 14, 40. If a plurality of semiconductors of the same kind are mounted, or a plurality of semiconductors 1A and 1B of different types are mounted, a circuit of a wide range can be formed to be small with a higher efficiency than when one semiconductor 1 is mounted. If the plurality of semiconductors are mounted, wiring between the semiconductor elements, i.e. ICs, becomes short to lower an impedance, whereby an electric high frequency transmission loss is reduced and an efficiency can be improved. When an electronic circuit module used in combination of a predetermined plurality of ICs is incorporated in one package, a ratio of a dead space decreases and the dead space becomes small. In other words, for example, in the case where two kinds of semiconductors for a transistor and for a diode are to be used, the semiconductors pair in terms of an electronic circuit are to be used, and therefore, leads

of the above one package can be reduced to three although the semiconductors in different packages ~~need~~ require five leads. The circuit of a large range can accordingly be formed to be small.

One example where the semiconductor package of the embodiment is applied to actual products, are power modules such as motors for industrial use, such as AC servo motors, usable for robots or component mounting apparatus. Specifically, such a motor has ~~the~~ a motor output of 100-200W, ~~the~~ a normal calorific value of 10-20W, ~~the~~ a load or abnormal calorific value of 20-100W or 20-200W, ~~performing~~ performs a switching conversion function of a semiconductor element at normal time and an accelerating and decelerating motion at loading time, and ~~causing~~ causes a locking motion of the motor's rotary shaft at abnormal time. In this case, each electrode has the following outer diameter and height: 1mm-diameter of each electrode at ~~the~~ a substrate side and ~~the~~ a semiconductor element side, 1mm-height at the substrate side, and 0.5mm-height at the semiconductor element side. The shape of each electrode is ~~column~~ a column. The load voltage of the semiconductor element is 200V, and the current is 1-5A. Taking into account ~~with~~ insulating properties, a distance between ~~the~~ adjacent electrodes having different potentials is ~~away from each other~~ by at least 0.4mm, and the electrodes are preferably coated with an insulating resin.

As above, according to the present invention, the

lower face electrodes of semiconductors, each having electrodes formed on both upper and lower faces, are joined with use of the solder to the radiating plate, and moreover, pillared or spherical electrodes are joined to the upper face electrodes of the semiconductor and the radiating plate. The semiconductor package constituted from one or a plurality of semiconductors can be formed in a simple structure with a superior heat radiation effect and of a stable quality.

Concretely, since the lower face electrodes of the semiconductors are joined to the radiating plate, heat generated at the semiconductors can be directly transmitted to the radiating plate. Moreover, the upper face first electrode (upper a electrode) and the upper face second electrode (upper b electrode) of the semiconductor are joined to the radiating plate with use of the pillared or spherical electrodes, which are thicker than a gold or aluminum wire used for wire bonding and are hard to deform after the joining. The other ends of the pillared (columnar) or spherical electrodes can be utilized as connecting parts to the circuit board. Accordingly, the present invention provides the semiconductor package which can cope with a large current, can easily improve the heat radiation efficiency and secure a distance between electrodes. The semiconductor of a large operating current and voltage, and a large heat amount, can be

mounted compactly, inexpensively and highly reliably, and can be manufactured stably.

When the semiconductor and the face of the radiating plate joined to the semiconductor are covered with the sealing resin in a manner to expose part of leading ends of the pillared or spherical electrodes, each component can be protected from deformation, damage, moisture, dust, and the like, and becomes easy to handle ~~with~~ as a semiconductor package after completion ~~completed~~.

When independent electric circuits of a plurality of polarities of a single or combination of gold, silver, copper, nickel, and tungsten are arranged ~~to the ceramic of the~~ on a ceramic radiating plate, and semiconductors of different kinds are joined to the ~~electric~~ circuits of the plurality of polarities of the radiating plate, the ~~independent~~ plurality of polarities can be formed independently of each other on the same face of the radiating plate 14 with the utilization of insulating properties, heat conduction, and heat radiation properties of the ceramic.

When the radiating plate is formed ~~in~~ of a multi-layer ceramic structure ~~of ceramic~~ having semiconductors, and electrodes for the pillared or spherical electrodes are formed of a single or combination of gold, silver, copper, nickel, and tungsten, on the front face thereof when the radiating plate has; and also ~~having~~ that of the conductive ~~conductor~~ layers, formed of the same material as ~~the material~~

of the electrodes on the front face, between the ceramic layers to be connected to the electrodes on the front face to radiate heat from both the ceramic radiating plate and the conductor layers, the heat generated at the semiconductors can be transmitted from the electric circuits through the conductive layers and internal conductors to a lower ceramic plate with utilization of heat conduction properties of the metal. Accordingly, heat diffusion efficiency is improved and heat radiation efficiency can also be improved.

In the case where one semiconductor is to be mounted, or a plurality of semiconductors having lower face electrodes of equal current and voltage characteristics are to be mounted, the radiating plate itself can be a conductor. If the radiating plate is formed of any one of copper, a copper alloy, aluminum, and an aluminum alloy, or the radiating plate is formed of this metal after being subjected to a surface treatment, the material forming the radiating plate transmits heat and electricity well, diffuses heat quickly and is easy to solder to other metals, so that the heat radiation effect for the semiconductors can further be effectuated.

When part of a sealing resin and part of the pillared or spherical electrodes are removed simultaneously after the pillared or spherical electrodes are covered with

the sealing resin, thereby exposing the electrode parts to form the connecting parts, the pillared or spherical electrodes can be uniformed accurately made in height ~~accurately~~.

When the pillared or spherical electrodes are pressed to be smooth after being joined to the semiconductors and the metallic radiating plate, or after being sealed with the sealing resin, the pillared or spherical electrodes are easily deformed to be uniform in height ~~easily~~ when pressured with use of a jig having a smooth face or a mold having a smooth face.

In the case where the pillared or spherical electrodes are formed of a ~~in the~~ double structure having a ~~of the~~ hard inside and soft outside, or of a ~~in the~~ double structure having the outside be of a material having a lower melting temperature than that of the material of the inside, although the soft outside of the pillared or spherical electrodes is deformed when joined to a the circuit board, the pillared or spherical electrodes are prevented from being largely deformed ~~large~~ as a whole because of being supported by the hard inside material, whereby a smoothness can be secured at the leading end parts of the pillared or spherical electrodes.

If a the radiating plate is provided with ~~the~~ pits and projections on a ~~to the front~~ face ~~of the face~~ opposite ~~to~~ a ~~the joined~~ face joined to ~~the~~ semiconductors, the radiating plate has a larger surface area, thus improving a the heat radiation effect and, also increasing a the contact area with ~~to the~~ air, thereby

increasing an amount of heat of the radiating plate ~~for radiating~~ radiated to the air. ~~The~~ Thus, the heat radiation effect can be promoted.

In an arrangement in which ~~the~~ a plurality of bumps are arranged ~~to~~ on each of ~~the~~ an upper face first electrode (upper a electrode) and ~~the~~ an upper face second electrode (upper b electrode) of ~~the~~ a semiconductor, with ~~the~~ pillared or spherical electrodes being joined ~~on~~ to the bumps, the semiconductor can be less damaged because the bumps are ~~the~~ small gold bumps ~~are~~ formed ~~through~~ via ultrasonic oscillation, ~~than~~ as opposed to when ~~the~~ large pillared or spherical electrodes are directly joined to the upper face first electrode (upper a electrode) and the upper face second electrode (upper b electrode) of the semiconductor. Setting the pillared or spherical electrodes on the bumps ~~through~~ via ultrasonic oscillation can ~~ease~~ lessen a load to the semiconductor because of the deformation of the bumps, and can adjust the height. ~~The~~ Gold bumps of the bumps are good in solderability, thereby enabling joining to the pillared or spherical electrodes ~~by~~ via a solder.

Although the present invention has been fully described in connection with the preferred embodiments thereof with reference to the accompanying drawings, it is to be noted that various changes and modifications are apparent to those skilled in the art. Such changes and modifications are to be understood as included within the

scope of the present invention as defined by the appended claims unless they depart therefrom.

ABSTRACT OF THE DISCLOSURE

Electrodes of one face of a semiconductor, which has electrodes formed ~~to~~ on both faces, and a heat radiating plate are directly joined to quickly absorb and diffuse heat of the semiconductor, thereby improving a heat radiation effect. At the same time, electrodes on an opposite face of the semiconductor are connected to projecting electrodes ~~with use of a wire~~ that are thicker than a wire for wire bonding and larger in current capacity. ~~and~~ These projecting electrodes can accordingly be utilized as ~~a~~ connecting terminals to a circuit board. Ceramic is used for the heat radiating plate, so that semiconductors of different functions can be mounted simultaneously.